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09/385,927	08/30/1999	FRED GRUNER	42390.P7268	9797

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EXAMINER	
WOOD, WILLIAM H	

ART UNIT	PAPER NUMBER
2124	23

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/385,927	Applicant(s) GRUNER ET AL.	
	Examiner William H. Wood	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20 and 23-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20 and 23-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 20 and 23-37 are pending and have been examined.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submissions filed on 10 October and 10 November 2003 has been entered.

Claim Rejections - 35 USC § 103

Claims 20 and 23-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Colavin** (USPN 5,666,115) in view of **Riffe** et al. (USPN 4,502,111) in further view of **Coon** et al. (USPN 5,619,666).

Claim 20

Colavin disclosed a method for aligning, the method comprising:

- inputting a stream into a second shifter *(figure 3, element 13)*, the stream being obtained exclusively from a first shifter *(figure 3, element 11)*;
- determining in a length decoder and in a first clock cycle, a length of a current [data element] *(figure 3, element 16)*;

- if a successive [data element] in the stream is contained in the second shifter then shifting the stream to a start of the successive [data element] based exclusively on the length of the current [data element], said shifting being performed during the first clock cycle and within the second shifter *(figure 3, elements 13 and 16; column 6, lines 47-65)*;

Colavin did not explicitly state *instruction* alignment and decoding. **Riffe** demonstrated that it was known at the time of invention to perform alignment of variable length instructions in instruction streams (column 1, lines 5-10). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the data alignment system of **Colavin** with performing alignment on instructions as the data as found in **Riffe**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide alignment of instructions and thus allowing a processor to quickly decode and execute those instructions by knowing the proper boundaries for instruction operation information (**Riffe**: column 1, lines 10-45).

Colavin did not explicitly state *if the successive instruction stream is not contained in the second shifter then shifting the successive instruction into the second shifter from the first shifter in the same clock cycle and shifting the instruction stream to the start of the successive instruction one clock cycle later.* **Riffe** demonstrated that it was known at the time of invention to make use of eight (8) byte rotators for instruction alignment (Figure 1, element 41). **Coon** demonstrated that it was known at the time of invention to make use of Intel architecture (IA) instruction set (column 5, lines 36-38), which can

have instructions varying up to 15 bytes. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the alignment system of **Colavin** with eight byte registers as found in **Riffe**'s teaching and IA as found in **Coon**. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide small shifters which save space on a processor and to provide service for a commonly known and thus easily implemented instruction set. Under such an implementation, the above limitation reads upon the cited prior art (if an instruction larger than the second register is found the first register will have to provide the result and using the first register will result in a clock delay before the shifting to the start of the next instruction, **Colavin**: figure 3).

Claim 23

Colavin and **Riffe** disclosed the method of claim 20, wherein the second shifter is connected to the length decoder via a latch *(**Colavin**: figure 3, element 22)*.

Claim 24

Colavin and **Riffe** disclosed the method of claim 20, wherein shifter is able to shift 8 bytes of data *(**Riffe**: Figure 1, element 41)*.

Claim 25

Colavin, **Riffe** and **Coon** disclosed the method of claim 20, wherein the first shifter is able to shift 16 bytes of data. **Colavin** demonstrated that it was known at the time of

invention to output of shifters is increasingly smaller (figure 3, outputs of elements 11 and 13). **Coon** demonstrated that it was known at the time of invention to make use of shifters if sixteen (16) bytes (column 6, lines 17-18) as common types of shifters. Official Notice is taken that it was known at the time of invention to use as little space as possible for components in logic. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the aligning and decoding system of **Colavin**, **Riffe** and **Coon** with a 16 byte shifter followed by a smaller eight byte shifter as suggested by **Colavin**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use the bare minimum in space needed and **Colavin** clearly needs more space for the first shifter that the second shifter, it is easy to implement commonly known types of shifters.

Claim 26

The limitations of method claim 26 correspond to method claim 20 and as such are rejected in the same manner.

Claim 27

Colavin, **Riffe** and **Coon** disclosed the method of claim 26, wherein the first and second shifters are connected in series and are synchronized to the same clock cycle *(**Colavin**: figure 3, clock)*.

Claim 28

Colavin, **Riffe** and **Coon** did not explicitly state the method of claim 27, wherein the first shifter has a capacity of 16 bytes and the second shifter has a capacity of 8 bytes. **Colavin** demonstrated that it was known at the time of invention to output of shifters is increasingly smaller (figure 3, outputs of elements 11 and 13). **Coon** demonstrated that it was known at the time of invention to make use of shifters if sixteen (16) bytes (column 6, lines 17-18) as common types of shifters. Official Notice is taken that it was known at the time of invention to use as little space as possible for components in logic. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the aligning and decoding system of **Colavin**, **Riffe** and **Coon** with a 16 byte shifter followed by a smaller eight byte shifter as suggested by **Colavin**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use the bare minimum in space needed and **Colavin** clearly needs more space for the first shifter that the second shifter, it is easy to implement commonly known types of shifters.

Claim 29

Colavin, **Riffe** and **Coon** disclosed the method of claim 26, wherein inputting the length of the first instruction comprises inputting said length directly from the length decoder to the second shifter *(**Colavin**: figure 3, elements 16 and 13)*.

Claim 30

Colavin, **Riffe** and **Coon** disclosed the method of claim 26, wherein the inputting the length of the first instruction comprises inputting said length from the length decoder to the first shifter via an intermediate latch *(**Colavin**: figure 3, elements 11 and 21)*.

Claim 31

Colavin disclosed logic for aligning, the logic comprising:

- a first shifter *(figure 3, element 11)*;
- a second shifter *(figure 3, element 13)*;
- a length decoder *(figure 3, element 16)*, wherein an output of the first shifter forms a direct input to the second shifter and exclusively defines data to be shifted therein *(figure 3, elements 11 and 13)*, an output of the second shifter is sent to the length decoder via an intermediate latch *(figure 3, element 22)*, and wherein a length of a current [data element] in the length decoder is directly input into the second shifter *(figure 3, elements 13 and 16)* and the second shifter shifts the data based exclusively on the length of the current instruction *(figure 3, elements 13 and 16)*.

Colavin did not explicitly state *instruction* alignment and decoding. **Riffe** demonstrated that it was known at the time of invention to perform alignment of variable length instructions in instruction streams (column 1, lines 5-10). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the data alignment system of **Colavin** with performing alignment on instructions as the data as found in **Riffe**'s teaching. This implementation would have been obvious because one of

ordinary skill in the art would be motivated to provide alignment of instructions and thus allowing a processor to quickly decode and execute those instructions by knowing the proper boundaries for instruction operation information (**Riffe**: column 1, lines 10-45).

Claim 32

Colavin, **Riffe** and **Coon** disclosed the logic of claim 31, wherein a length of the current instruction in the length decoder is input into the first shifter via an intermediate latch *(**Colavin**: figure 3, element 21).*

Claim 33

Colavin, **Riffe** and **Coon** did not explicitly state the logic of claim 31, wherein the first shifter has a greater shifting capacity than the second shifter. **Colavin** demonstrated that it was known at the time of invention to output of shifters is increasingly smaller (figure 3, outputs of elements 11 and 13). Official Notice is taken that it was known at the time of invention to use as little space as possible for components in logic. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the aligning and decoding system of **Colavin**, **Riffe** and **Coon** with a larger shifter followed by a smaller shifter as suggested by **Colavin**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use the bare minimum in space needed and **Colavin** clearly needs more space for the first shifter that the second shifter.

Claim 34

Colavin, **Riffe** and **Coon** disclosed the logic of claim 31, wherein the first shifter has a capacity of 16 bytes and the second shifter has a capacity of 8 bytes *(see claim 28's rejection)*.

Claims 35-37

The limitations of logic claims 35-37 correspond to the limitation of logic claims 31-34 and are rejected in the same manner.

Response to Arguments

Applicant's arguments with respect to claims 20 and 23-37 have been considered but are moot in view of the new ground(s) of rejection.

The rejections based on 35 U.S.C. § 112 of claim 20 in the previous office action (mailed 12 August 2003) are withdrawn.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
February 6, 2004

TODD INGBERG
PRIMARY EXAMINER